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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,048	04/08/2004	Sadanand V. Deshpande	FIS920030397US1	3047

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EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,048	DESHPANDE ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The request for continued examination filed on 30 May 2006 has been entered and made of record.

2. The amendments to claims 1, 2, and 8 have been entered and the objection to claim 2 has been withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1, 6-8, and 13-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Pradeep (US 6,316,304).

5. Regarding claims **1 and 8**, Pradeep discloses in Figure 8 an integrated circuit structure comprising: a substrate (30); first-type transistors (46) on said substrate, wherein said first-type transistors comprise first gate conductors (34) and first spacers (36) adjacent said first gate conductors; second-type transistors (48) on said substrate, wherein said second-type transistors comprise second gate conductors (35), said first spacers (36) adjacent said second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer (38) on said first spacers, and second spacers (40/44) on said etch stop layer; first-type impurity implants (50) in areas of said

substrate completely outside of said first spacers of said first gate conductors (34); second-type impurity implants (50) in areas of said substrate completely outside of said second spacers of said second gate conductors (35); first silicide regions proximate said first spacers of first-type transistors (col 4 ln 31-34); and second silicide regions proximate said second spacers of said second-type transistors (col 4 ln 31-34), wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors (col 3 ln 63-67, two spacer widths *w* and *W*).

6. With regards to claims **6 and 13**, Pradeep discloses in Fig 9 the structure of claims 1 and 8, wherein said first type impurity and said second type impurity comprises source/drain impurities (50).

7. Regarding claims **7 and 14**, Pradeep discloses in Fig 9 the structure of claims 1 and 8, wherein said first type transistors (46n) comprise NFETs and said second type transistors (48p) comprise PFETs.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **2-3 and 9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pradeep in view of Kao (US 6,500,765).

10. Regarding claims **2-3 and 9-10**, Pradeep discloses in Fig 8 the circuit of claims 1 and 8, but fails to specify that the second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors. Pradeep also fails to specify that the etch stop layer is only on said first spacers that are adjacent said second gate conductors, and not on the first spacers of the first gate conductors.

Kao teaches the enlargement of distance between source and drain, using the spacer thickness (see Fig 5), in order to control the diffusion rate of different FET devices (col 3 ln 10-30). Where the diffusion rate is fast the spacer width is relatively thick. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Kao on the device of Pradeep, omitting the etch stop layer and second spacer from slow diffusion transistors, while maintaining the etch stop layer and second spacer on fast diffusion transistors.

11. Claims **4-5 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pradeep in view of Ju.

12. Regarding claim **4**, Pradeep discloses in Figure 8 the circuit of claims 1 and 8 as discussed above. Pradeep fails to specify first-type impurity implants in areas of said substrate adjacent said first spacers of said first gate conductors; and second-type impurity implants in areas of said substrate adjacent said second spacers of said second gate conductors.

Ju teaches in Fig 5 first and second offsets for different types of transistors, where first impurities (20) are implanted adjacent the first transistor spacers and second impurities (26) are adjacent the second spacers, in order to optimize the gate to drain overlap capacitance (col 2 ln 17-18) by spacing the p-type impurities further from the gate. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ju on the structure of Pradeep to optimize gate to drain capacitance.

13. With regards to claims **5 and 12**, Ju discloses in Figure 5 the structure of claims 4 and 8, wherein said first type impurity (20) is spaced closer to said first gate conductors than said second type impurity (26) is spaced from said second gate conductors.

Response to Arguments

14. Applicant's arguments with respect to claims 1-10 and 12-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

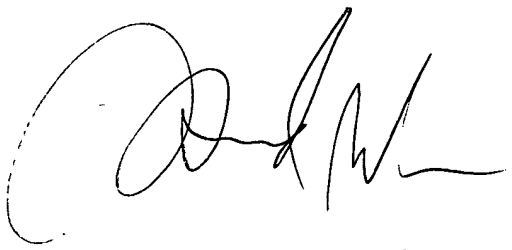
Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John C Ingham
Examiner
Art Unit 2814

jci



HOWARD WEISS
PRIMARY EXAMINER